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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,863	10/11/2004	David C. H. Cheng	14098-US-PA	5862

31561 7590 05/31/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
NORRIS, JEREMY C	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,863	CHENG, DAVID C. H.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The

abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because of the use of the phrase "is provided". Correction is required. See MPEP § 608.01(b). The Examiner suggests simply deleting this phrase.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 6, and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by US 3,148,310 (Feldman).

Feldman discloses, referring primarily to figure 4, a method of forming conductive column in a fabrication of a circuit board, the circuit board comprising a dielectric layer (41) formed thereon, the method comprising: forming a first blind hole in a first surface of the dielectric layer; forming a second blind hole in a second surface of the dielectric layer opposite to the first surface, a blind end of the first blind hole connecting to a blind end of the second blind hole, the first blind hole and the second blind hole constituting a through hole (43, col. 6, lines 50-60), wherein an inner diameter of the through hole near the first surface or the second surface is substantially larger than an inner diameter

of the through hole near a middle portion of the through hole (col. 6, lines 40-45); and filling a conductive material (46) in the through hole to form a conductive column (col. 6, lines 50-60) [claim 1], wherein the first blind hole and the second blind hole have a cone shape, and the through hole and the conductive column have an hourglass shape (col. 6, lines 40-45) [claim 2], wherein the first blind hole is formed by a mechanical drilling method (col. 6, lines 50-55) [claim 5], wherein the second blind hole is formed by a mechanical drilling method (col. 6, lines 50-55) [claim 6], wherein the step of filling the conductive material comprises plating process (col. 6, lines 55-60) [claim 9], wherein the conductive material fills the through hole from a position where the blind ends of the first and second blind holes connect with each other in the through hole and extends towards the first surface and or the second surface (col. 6, lines 60-65) [claim 10].

Similarly, Feldman discloses, a circuit board, comprising: a dielectric layer (41), having a first surface, a second surface opposite to the first surface and at least one through hole (42), wherein the through hole passes through the dielectric layer, and an inner diameter of the through hole near the first or the second surface is substantially larger than an inner diameter of the through hole near a middle portion of the through hole (col. 6, lines 40-45); and at least one conductive column (46), disposed in the through hole, a shape of the conductive column being substantially consistent to a shape of the through hole [claim 11], wherein the through hole and the conductive column have an hourglass shape (col. 6, lines 40-45) [claim 12].

Claims 1-4 and 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by US 3,354,543 (Lawrence).

Lawrence discloses, referring primarily to figures 2a-e, a method of forming conductive column in a fabrication of a circuit board, the circuit board comprising a dielectric layer (col. 3, lines 60-70) formed thereon, the method comprising: forming a first blind hole (34B) in a first surface of the dielectric layer; forming a second blind hole (36B) in a second surface of the dielectric layer opposite to the first surface, a blind end of the first blind hole connecting to a blind end of the second blind hole, the first blind hole and the second blind hole constituting a through hole (24B), wherein an inner diameter of the through hole near the first surface or the second surface is substantially larger than an inner diameter of the through hole near a middle portion of the through hole (col. 2, lines 60-65); and filling a conductive material (col. 6, lines 1-15) in the through hole to form a conductive column [claim 1], wherein the first blind hole and the second blind hole have a cone shape, and the through hole and the conductive column have an hourglass shape (col. 2, lines 65-70) [claim 2], wherein the circuit board further comprises a first conductive layer (12B) disposed over the first surface of the dielectric layer, and after forming the first blind hole in the dielectric layer, the first blind hole is passed through the first conductive layer [claim 3], wherein the circuit board further comprises a second conductive layer (16B) disposed over the second surface of the dielectric layer, and after forming the second blind hole in the dielectric layer, the second blind hole is passed through the second conductive layer [claim 4] wherein the step of filling the conductive material comprises plating process (col. 6, lines 1-15)

[claim 9], wherein the conductive material fills the through hole from a position where the blind ends of the first and second blind holes connect with each other in the through hole and extends towards the first surface and or the second surface (col. 6, lines 1-15) [claim 10].

Similarly, Lawrence discloses, a circuit board, comprising: a dielectric layer (col. 3, lines 60-70), having a first surface, a second surface opposite to the first surface and at least one through hole (24B), wherein the through hole passes through the dielectric layer, and an inner diameter of the through hole near the first or the second surface is substantially larger than an inner diameter of the through hole near a middle portion of the through hole (col. 2, lines 65-70); and at least one conductive column (col. 6, lines 1-15), disposed in the through hole, a shape of the conductive column being substantially consistent to a shape of the through hole [claim 11], wherein the through hole and the conductive column have an hourglass shape (col. 2, lines 65-70) [claim 12].

Additionally, Lawrence discloses, a circuit board, comprising: a dielectric layer (col. 3, lines 60-70), having a first surface and a second surface opposite to the first surface; and a first conductive layer (12B), disposed over the first surface of the dielectric layer, wherein a through hole (24B) is formed in the first dielectric layer and the first conductive layer passing through the dielectric layer and the first conductive layer, and an inner diameter of the through hole near the first or the second surface is substantially larger than an inner diameter of the through hole near a middle portion of the through hole (col. 2, lines 65-70); and at least one conductive column (col. 6, lines

1-15), disposed in the through hole, a shape of the conductive column being substantially consistent to a shape of the through hole [claim 13], wherein the through hole and the conductive column have an hourglass shape (col. 2, lines 65-70) [claim 14], further comprising a second conductive layer (16B) disposed over the second surface of the dielectric layer, and wherein the through hole passes through the second conductive layer [claim 15].

Claims 1, 2, and 7-12 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,232,548 (Ehrenberg).

Ehrenberg discloses, referring primarily to figures 1-4 and 5B, a method of forming conductive column in a fabrication of a circuit board, the circuit board comprising a dielectric layer (14) formed thereon, the method comprising: forming a first blind hole in a first surface of the dielectric layer; forming a second blind hole in a second surface of the dielectric layer opposite to the first surface, a blind end of the first blind hole connecting to a blind end of the second blind hole, the first blind hole and the second blind hole constituting a through hole (16, col. 5, lines 20-40), wherein an inner diameter of the through hole near the first surface or the second surface is substantially larger than an inner diameter of the through hole near a middle portion of the through hole (figure 4); and filling a conductive material (26) in the through hole to form a conductive column [claim 1], wherein the first blind hole and the second blind hole have a cone shape, and the through hole and the conductive column have an hourglass shape (figure 4) [claim 2], wherein the first blind hole is formed by a laser drilling method

(col. 5, lines 20-25) [claim 7], wherein the second blind hole is formed by a laser drilling method (col. 5, lines 20-25) [claim 8] wherein the step of filling the conductive material comprises plating process (col. 5, lines 50-60) [claim 9], wherein the conductive material fills the through hole from a position where the blind ends of the first and second blind holes connect with each other in the through hole and extends towards the first surface and or the second surface (col. 6, lines 55-60) [claim 10].

Similarly, Ehrenberg discloses, a circuit board, comprising: a dielectric layer (14), having a first surface, a second surface opposite to the first surface and at least one through hole (16), wherein the through hole passes through the dielectric layer, and an inner diameter of the through hole near the first or the second surface is substantially larger than an inner diameter of the through hole near a middle portion of the through hole (figure 4); and at least one conductive column (26), disposed in the through hole, a shape of the conductive column being substantially consistent to a shape of the through hole [claim 11], wherein the through hole and the conductive column have an hourglass shape (figure 4) [claim 12].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following documents disclose PCBs having generally hourglass shaped vias:

US 6,211,468 B1 Windschitl,

US 6,274,820 B1 DiStefano et al.,

US 6,486,394 B1 Schmidt et al..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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